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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,699	10/21/2003	Kiran V. Chatty	BUR920030120US1	2698

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EXAMINER	
VU, DAVID	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,699	CHATTY ET AL.	
	Examiner	Art Unit	
	DAVID VU	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) *32-51* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-51* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-10 and 15-31 are rejected under 35 U. S. C. 102(b) as being anticipated by Kim et al. (US Pat. 5,675,170).

Regarding claims 1 and 22, Kim discloses, in figs. 3 and 4, a method of forming a CMOS semiconductor structure having improved latch-up robustness, the method comprising the steps of: providing a substrate 1 including an injection site (I/O) and a plurality of a CMOS circuit structures (NMOS/PMOS), wherein at least one of circuit structures has a susceptibility to a latch-up condition (col. 3, lines 8-16); and forming a plurality of contact regions (22/23/41/32/33/2/3/4) inter-spaced a varying distance between circuit structures.

Regarding claims 2, 3, 23 and 24, Kim discloses the distance varies with the proximity of contact regions to injection site; wherein distance varies with the susceptibility of circuit structures to a latch-up condition (figs. 3-4 and col. 3, lines 8-16).

Regarding claims 4-6 and 25-27, Kim discloses the plurality of contact regions comprises a first contact region 22 and a second contact region 23 spaced a first distance apart, and second

contact region 23 and a third contact region 41 spaced a second distance apart different from first distance (figs. 3-4).

Regarding claim 7, Kim discloses the substrate comprises a well region having formed therein latch-up susceptible circuit structure (figs. 3-4).

Regarding claim 8, Kim discloses the well region (3/4) is n-type (figs. 3-4).

Regarding claim 9, Kim discloses the n-type well region (3/4) includes at least one contact comprising an n+ region (41/34) (figs. 3-4).

Regarding claim 10, Kim discloses at least one contact is coupled to Vdd (figs. 3-4).

Regarding claim 15, Kim discloses the plurality of contact regions are located along an axis and arranged vertically relative to axis (fig. 3).

Regarding claim 16, Kim discloses the plurality of contact regions are located along an axis and arranged horizontally relative to axis (fig. 3).

Regarding claim 17, Kim discloses the plurality of contact regions are located along an axis and arranged concentrically relative to axis (fig. 3).

Regarding claims 20 and 30, Kim discloses the distance increases as the distance of plurality of contact regions from injection site increases (figs. 3 and 4).

Regarding claims 21 and 31, Kim discloses the plurality of contact regions are located along an axis so that spacing between adjacent contact regions increases as the distance from injection site increases (figs. 3 and 4).

Regarding claims 18, 19, 28 and 29, the limitations " wherein said distance is determined such that ...." (claims 18 and 28) or " wherein said external current injector is a cable discharge ...." (claims 19 and 29) are merely functional/intended use limitations that do not structurally

distinguish the claimed invention over the prior. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See In re Casey, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and In re Otto, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963).

2. Claims 1, 7 and 11-14 are rejected under 35 U. S. C. 102(b) as being anticipated by Magee (US Pat. 4,642,667).

Regarding claim 1, Magee discloses, in figs. 1 and 2, a method of forming a semiconductor structure having improved latch-up robustness, the method comprising the steps of: providing a substrate 11 including an injection site (I/O) and a plurality of circuit structures (CMOS), wherein at least one of circuit structures has a susceptibility to a latch-up condition (col. 1, line 62 through col. 2, line 53); and forming a plurality of contact regions (32/33/34/35/36) inter-spaced a varying distance between circuit structures.

Regarding claims 7 and 11, Magee discloses, in figs. 1 and 2, substrate comprises a p-well region having formed therein latch-up susceptible circuit structure.

Regarding claim 12, Magee discloses, in figs. 1 and 2, a p-type well region includes at least one contact comprising a p+ region.

Regarding claim 13, Magee discloses, in figs. 1 and 2, at least one contact is coupled to ground.

Regarding claim 14, Magee discloses, in figs. 1 and 2, at least one contact is coupled to Vss.

Response to Arguments

3. Applicant's arguments filed 09/14/05 have been fully considered but they are not persuasive.

4. Applicant argues that Kim and Magee are not anticipatory as it does not applicable to modern CMOS semiconductor structures. However, this argument is not persuasive. Kim discloses, in figs. 3 and 4, a plurality of a CMOS circuit structures (NMOS/PMOS) (col. 1, lines 13-14), wherein at least one of circuit structures has a susceptibility to a latch-up condition (col. 3, lines 8-16 7& Abstract). Magee discloses that "The structure is compatible with conventional CMOS and NMOS processing techniques" (See Abstract). As such, applicant's argument that Kim and Magee fails to anticipate claim 1-31 is not persuasive.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (571) 272-1798. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm. If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Vu

November 27, 2005.